Using Finite Element Method software to enhance teaching about copper pillar bump flip-chip packaging

Yunn-Horng Guu, Lung-Sheng Lee & Ming-Zheng Huang

National United University
Miaoli, Taiwan

ABSTRACT: This study uses Finite Element Method (FEM) software to analyse the mechanical behaviour of copper pillar bump flip-chip packaging when subjected to temperature loading. The major advantages of FEM software are that they can simulate the robustness and performance of components and assemblies, as well as enable mechanical engineering students to understand the details of the planning, design and analysis of packaging better. The proposed simulation analysis of the flip-chip packaging is suitable for the courses related to Computer-Aided Engineering (CAE) and electronic packages for junior and senior university students.

INTRODUCTION

Flip-chip technology is widely used in the electronic packaging industry due to its advantages, such as high I/O density capability, excellent electrical performance due to the shorter electrical connections between the chip and substrate, high-speed transmission, superior heat dissipation, low cost and high reliability [1-3]. Pillar bump is the key component for flip-chip interconnection, which connects the die to the substrate via a co nductive bump [4]. The fine-pitch of interconnection can be achieved by using copper pillar bumps because they have a high aspect ratio [5]. As compared with the conventional high-lead SnPb solder bump, the copper pillar bump possessed greater conductive capacity, efficient thermal performance and improved resistance to electromigration [6]. The pillar bump with a Cu base and eutectic solder cap had a higher resistance to fatigue failure in comparison with a pure eutectic solder bump [7].

The mechanical behaviour of the flip-chip packaging is a crucial issue in the packaging industry, and it is also related to the reliability of electronic devices. The measurement of the stress or deformation in packaging was a difficult and tedious job, therefore, many researchers adopted FEM to study packaging. Kim and Jung used the finite element analysis tool, ANSYS, to analyse the electronic packages. The stress and equivalent plastic strain were performed to interpret the failure mechanisms [8]. Lin et al investigated the stress development at the interfaces of the die/underfill by means of finite element analysis, and demonstrated that the geometrical parameters and materials were significant for the reliability of the OM-FC packaging [9]. Tsai and Chang employed FEM to simulate the warping of flip-chip PBGA packaging under heating and cooling conditions [10]. Chen and Lin employed finite element analysis to investigate the failure mechanism and studied the optimisation of the copper pillar bump.

The finite element simulation results indicate that the copper pillar bump sustained the largest tensile stress during the temperature cycling test. The larger diameter copper pillar bump can reduce the tensile stress significantly at the high temperature environment [11]. Zhang et al established the finite element models to study the detailed Cu/LowK structure in the chip and found that the stress in post flip-chip attachment process is significantly higher than that after full assembly [12]. Wang et al applied a three-dimensional simulation approach to explore the underfill process in flip-chip encapsulation. The simulation provided a promising solution for the microchip encapsulation process [13-15].

The major challenge with flip-chip packaging technology originated from thermal stresses, which are caused by the CTE (coefficient of thermal expansion) mismatch [16]. The design of the flip-chip structure and stress analysis are essential steps in the packaging technology due to their significant impact on the reliability of the electronic devices. The authors assume that the computer software used in the analysis of electronic packaging may allow students to visualise the physical phenomena of the structure and obtain an improved understanding. The purpose of this study is to use the FEM software ANSYS to simulate the thermally induced deformations and stresses of flip-chip ball grid array (BGA) packages with a copper pillar bump.

COPPER PILLAR BUMP FLIP-CHIP PACKAGING

The configuration of copper pillar flip-chip packaging in this study is shown in Figure 1. The copper pillar bump is cylindrical with a solder cap instead of the traditional solder bump connecting to the silicon die and substrate. The chip (die) size of the specimen is 5 mm× 5mm× 0.785mm with a 162 μm bump pitch. The dimension of the substrate is 31 mm × 31 mm × 1.05 mm. The underfill layer height is 76μm. Figure 2 shows the cross-section of the copper pillar bump. The copper post height and diameter are 50 μm and 90 μm, respectively.

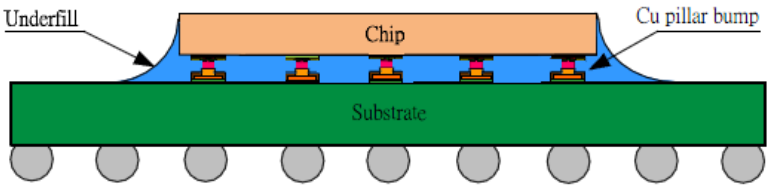


Figure 1: Configuration of copper pillar bump flip-chip packaging.

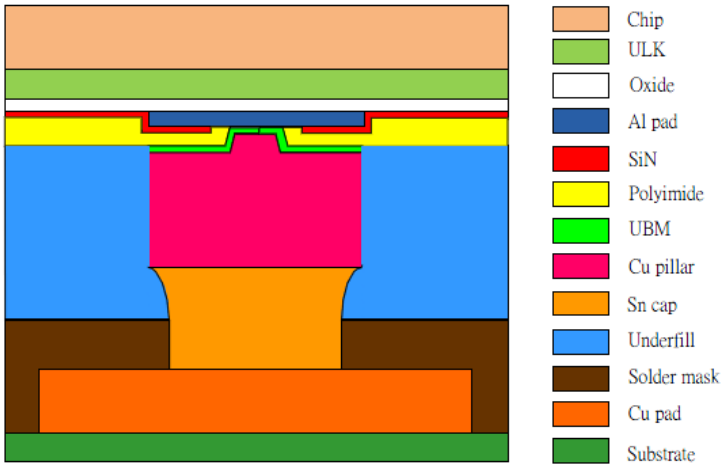


Figure 2: Cross section of the copper pillar bump.

FEM ANALYSIS

The commercial program ANSYS was employed to evaluate the thermally induced deformations and stresses of the flip-chip packaging. A three-dimensional elastic analysis was conducted in this study. The analytical steps of FEM are schematically illustrated in Figure 3.

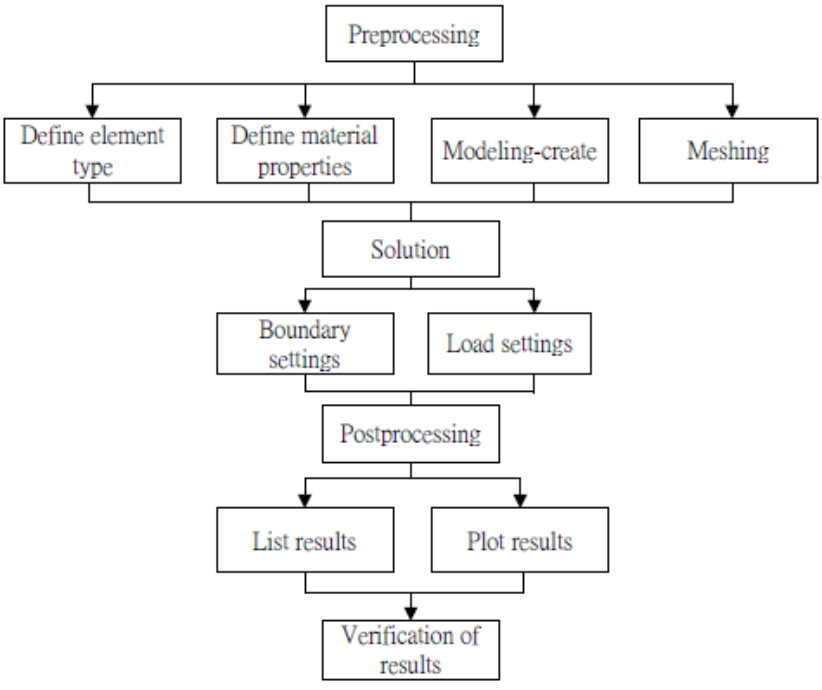


Figure 3: Basic processes of FEM.

The pre-processing phase includes defining the element, setting material attributes, modelling and meshing. The solution phase comprises of boundary conditions, initial conditions and loading setting. The post-processing phase consists of computational processing and graphical results. Finally, the verification was conducted to ensure the validity of the analytical results. Only a half section of the test specimen was analysed due to geometrical symmetry. The finite element model of the flip-chip packaging is illustrated in Figure 4.

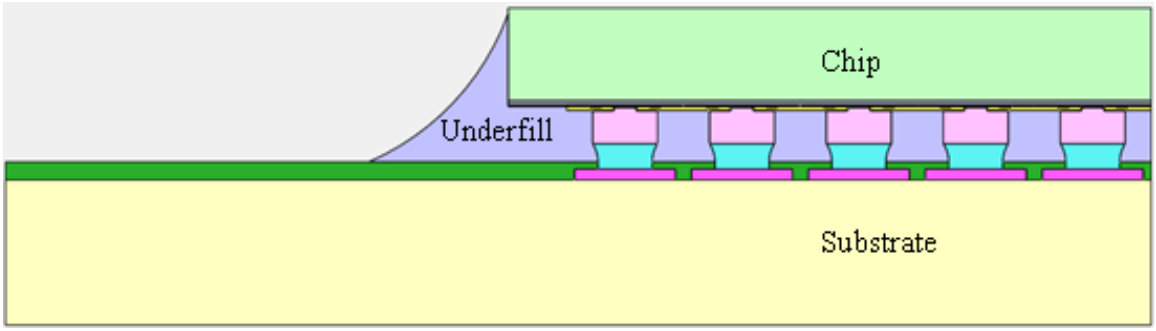


Figure 4: Finite element model.

A three-dimensional solid element (Solid 185) with eight-node brick elements were chosen for the finite element analysis. Figure 5 shows the finite element mesh of the copper pillar bump. The fine local mesh appears near the bumps. Mesh refinement was implemented to conduct convergence analysis to ensure the validity of the analytical results.

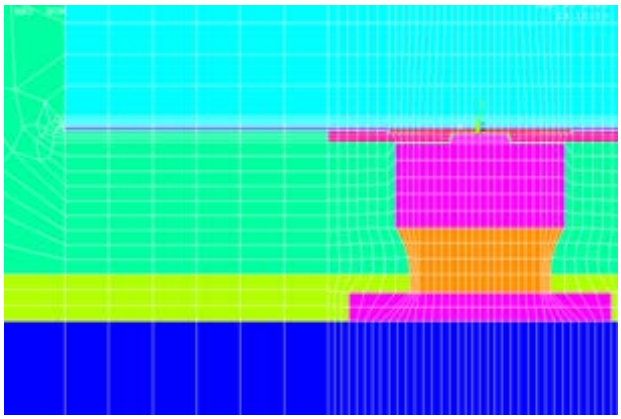


Figure 5: Copper pillar bump mesh.

Table 1 lists the material properties of the copper pillar bump flip-chip packaging. All the material properties of the components, except the solder ball, are assumed to be linear-elastic, homogeneous and isotropic.

Table 1: Material properties of copper pillar bump flip-chip packaging.

Items	Young's modulus (GPa)	CTE (ppm/^{0}C)	Poisson's ratio	T_g (^{0}C)
Silicon die	131	2.8	0.278	
Oxide	72	0.5	0.16	
Al pad	71	23	0.33	
SiN	270	5	0.28	
Polyimide	3.5	35	0.35	
UBM	135	14.5	0.33	
Sn cap	59@-55 ^{0}C, 45@40 ^{0}C, 28@135 ^{0}C	22	0.35	
Copper pillar/ Copper pad	121	16.3	0.34	
Solder mask	3.5	42/98 (under T_g/over T_g)	0.43	120
Substrate	26	12.4	0.22	
Underfill	Uf1/UF2 (under T_g/over T_g)	α 1/ α 2 (under T_g/over T_g)	Uf ν	100

Figure 6 shows the applied boundary constraints. The packaging model is fixed at point A. The packaging is subjected to thermal load cooling from 165 ^{0}C to -55 ^{0}C. The stress-free state is set at 165 ^{0}C, which is the underfill curing temperature.

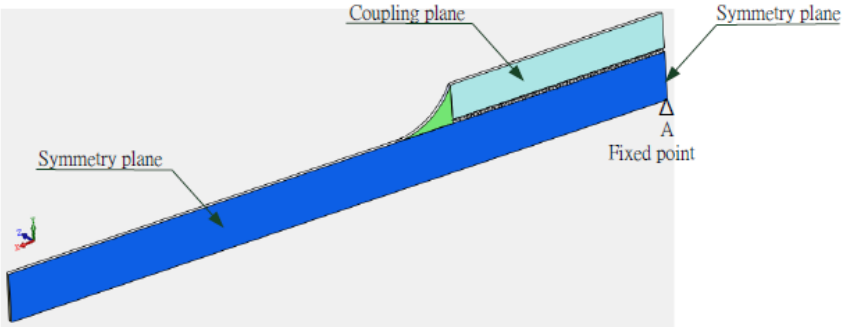


Figure 6: Finite element boundary conditions.

In this study, perfect bonding is assumed at all interfaces between various materials, while no void exists in the solder ball. Once the above pre-processing, boundary settings and load settings were completed, the students could solve the packaging using FEM software and, subsequently, observe the analytical results through graphical displays and tabular listings, which include the deformed shape, displacements and stresses. Finally, the students use the equilibrium conditions or the conservation of energy to confirm the validity of the results. The experimental verification of a finite element model is the ideal way to assess the validity of the results, when economically feasible or practical.

RESEARCH RESULTS AND DISCUSSIONS

Deformations of the Flip-chip Packaging

The flip-chip packaging is composed of several materials, which have distinct CTEs. The thermal deformation is caused by the unmatched CTE of the materials. The deformation induced by a CTE mismatch was evaluated by the FEM software. Figure 7 depicts the effects of temperatures on the deformation of the flip-chip packaging.

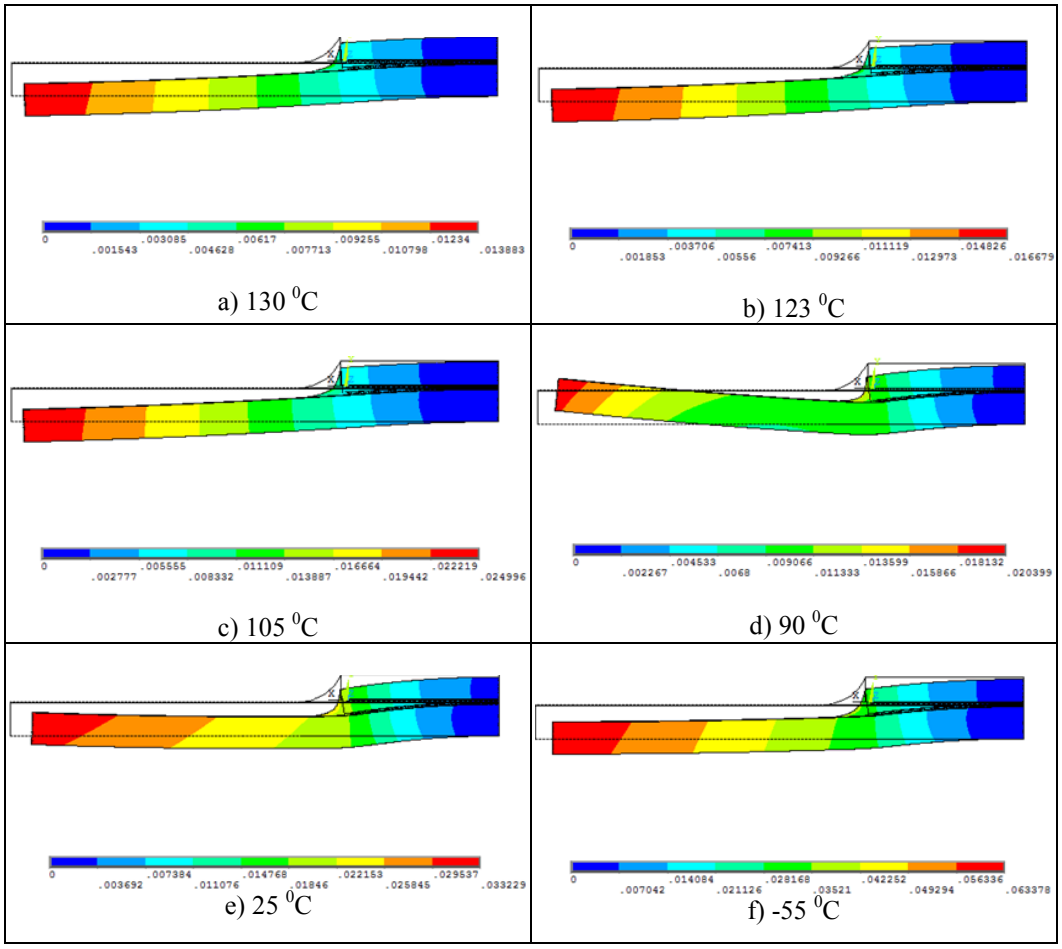


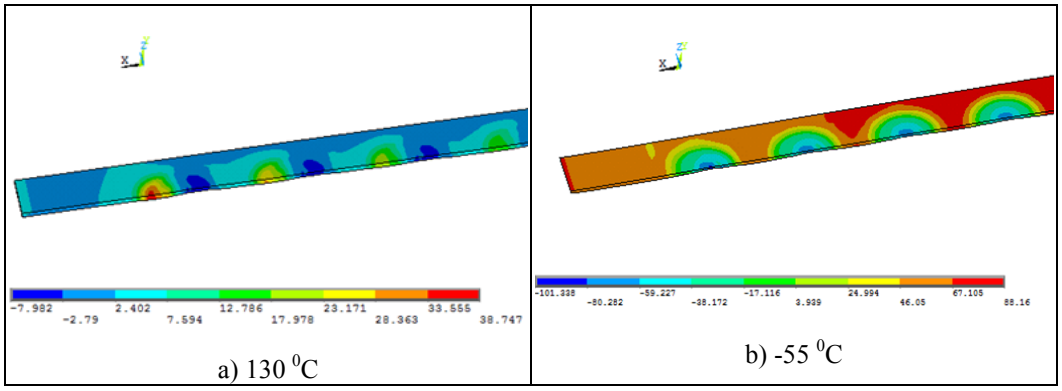
Figure 7: The deformations of the flip-chip packaging under various temperatures.

Figures 7a, 7b and 7c show the deformations of the flip-chip packaging at the temperatures of 130 ^{0}C, 123 ^{0}C, and 105 ^{0}C, respectively. The maximum vertical displacements at the free end are -13.88 µm, -16.67 µm, and -24.99 µm. The shape of packaging is concave downward. The extent of the concave downward shape of the packaging increases as the temperature gradient increases. The deformation at the temperature of 90 ^{0}C is illustrated in Figure 7d.

The maximum vertical displacement at free end is 20.39 µm. The shape of the packaging created a phenomenon of concave upward. This phenomenon is attributed to the temperature decreasing to the under fill glass transition temperature of 100 ^{0}C, while the Young's modulus of under fill varied from 0.09GPa to 10.70GPa. The under fill generated stress while solidified to pull the substrate, eventually leading to a change in the shape of the substrate from concave downward to concave upward.

Figures 7e and 7f show the deformations of the flip-chip structure at the temperatures of 25 ^{0}C and -55 ^{0}C. These graphs indicate that the maximum vertical displacements at the free end are -33.22 µm and -63.37 µm.

A comparison of Figures 7a - 7c and Figures 7e - 7f reveals that the vertical displacement increases as the temperature gradient increases, as a high temperature gradient causes a steep thermal deformation within the flip-chip structure. Furthermore, the under fill can reduce the influence of the heat load between the chip and substrate. Based on the numerical and graphical outcomes obtained from the software, the students were able to understand flip chip packaging and interpret the obtained data as long as they paid attention.

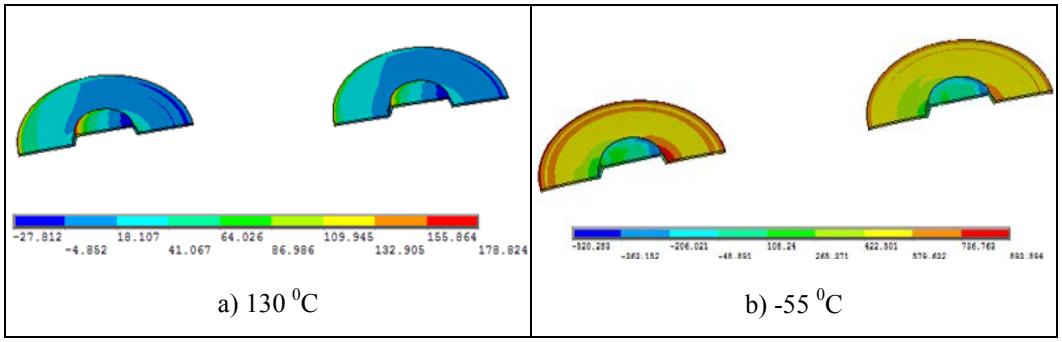


a) 130 ^{0}C b) -55 ^{0}C

Figure 8: The stresses of ULK at the temperature of 130 ^{0}C and -55 ^{0}C.

Stresses of the Flip-chip Packaging

Figure 8 shows the stresses distribution of ULK at the temperatures of 130 ^{0}C and -55 ^{0}C. It was found that, at the temperature of 130 ^{0}C, the maximum principal stress was 38.75 MPa. When the temperature drops to -55 ^{0}C, the maximum principal stress of ULK became 88.16 MPa. The nearer fixed end has a greater stress on the structure.

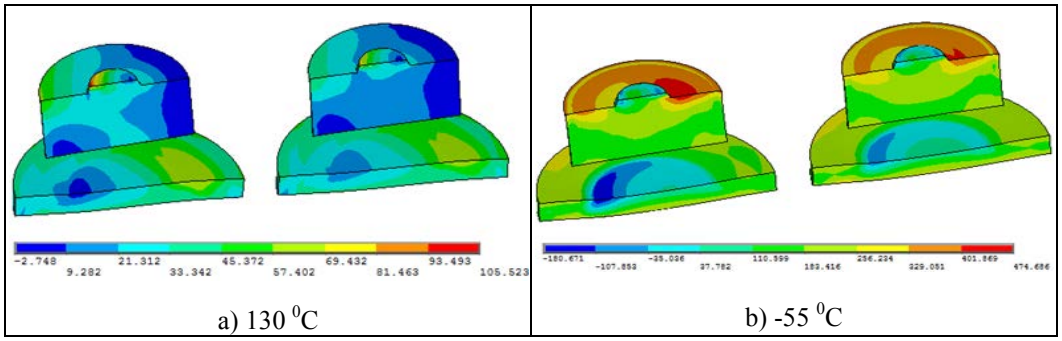


a) 130 ^{0}C b) -55 ^{0}C

Figure 9: The stresses of UBM at the temperature of 130 ^{0}C and -55 ^{0}C.

Figure 9 depicts the stresses of UBM of the flip-chip packaging. At the temperature of 130 ^{0}C, the maximum stress of 178.82 MPa was found on the UBM. When the temperature decreased to -55 ^{0}C, the UBM of the flip-chip structure exhibited greater stress (893.89 MPa). This is because of a higher temperature gradient in the structure, which prompted a larger deformation in the packaging and, hence, increased the stress.

Figure 10 illustrates the stresses of the copper pillar bump. The simulation results indicate that the maximum stress increased as a decreasing temperature gradient was applied. The location of the maximum principal stress of the copper pillar bump was the same as UBM. The software tool enabled the students to learn and understand the mechanic behaviour of flip-chip packaging. Through FEM software, the design parameters and process conditions can be quickly and efficiently verified, compared to physical prototyping.



a) 130 ^{0}C b) -55 ^{0}C

Figure 10: The stresses of the copper pillar bump at the temperature of 130 ^{0}C and -55 ^{0}C.

CONCLUSIONS

The measurement of deformation and stress of the flip-chip packaging was difficult to obtain. This study introduced a powerful FEM software, which allowed students to evaluate the deformation and stress characteristics of the flip-chip packaging caused by temperature. According to the simulation results, the following conclusions could be made:

1. The maximum vertical displacement occurred at the free end of the flip-chip packaging.
2. The extent of concave downward of the flip-chip packaging increases with the increasing temperature gradient. A large temperature gradient is associated with a larger concave downward.
3. The under fill can reduce the influence of the heat load between the chip and substrate.
4. The nearer fixed end of packaging ULK has a greater stress.
5. The software's graphical illustrations significantly increased the motivation of students for future study.

ACKNOWLEDGEMENTS

This research was sponsored by the National Science Council (NSC), Taiwan, under contract No: NSC 100-2511-S-239-002.

REFERENCES

1. Huang, M., Yeow, O.G., Poo, C.Y. and Jiang, T., A study on copper pillar interconnect in flip-chip-on-module packaging. *Proc. 9th Electronics Packaging Technol. Conf.*, 325-330 (2007).
2. Yu, J., Anand, A., Mui, Y.C., Srinivasan, P. and Master, R., Reliability study on copper pillar bumping with lead free solder. *Proc. 9th Electronics Packaging Technol. Conf.*, 618-622 (2007).
3. Vardaman, E.J., New developments in Flip chip. *Proc. IEEE 9th VLSI Packaging Workshop, Japan*, 99-101 (2008).
4. Lau, J.H., *Flip Chip Technologies*. New York: McGraw-Hill (1995).
5. Lee, M.T., Huang, J.P., Lin, G.T., Lin, Y.H., Jiang, Y.J., Chiu, S. and Huang, C.M., Optimization of copper pillar bump design for fine pitch flip-chip packages. *Proc. IMPACT Conf. 2009 Inter. 3D IC Conf.*, 128-131 (2009).
6. Joachim Kloeser, E-A.W., High performance flip-chip packages with copper pillar bumping, *Global SMT & Packaging*, 28-31 (2006).
7. Wang, T., Tung, F., Foo, L. and Dutta, V., Studies on a novel flip-chip interconnect structure-Pillar bump. *Proc. 51st Electronic Components and Technol. Conf.*, 1-8 (2001).
8. Kim, J-W. and Jung, S-B., Optimization of shear test for flip chip solder bump using 3-dimensional computer simulation. *Microelectron Engng.*, 82, 554–560 (2005).
9. Lin, Y. and Shi, F.G., Package design and materials selection optimization for overmolded flip chip packaging. *IEEE Transactions on Adv. Packaging*, 29, **3,** 525-532 (2006).
10. Tsai, M.Y. and Chang, H.Y., Warpage measurement and simulation of Flip-Chip PBGA package under thermal loading. *Proc. 2008 10th Inter. Conf. on Electronic Materials and Packaging*, 145-148 (2008).
11. Chen, K.M. and Lin, T.S., Copper pillar bump design optimization for lead free flip-chip packaging. *J. Mater. Science: Mater. El.,* 21, **3**, 278-284 (2010).
12. Zhang, X.R., Zhu, W.H., Liew, B.P., Gaurav, M., Yeo, A. and Chan, K.C., Copper pillar bump structure optimization for flip chip packaging with Cu/Low-K stack. *Proc. 2010 11th Inter. Conf. on Thermal, Mechanical and Multi-Physics Simulation, and Experiments in Microelectronics and Microsystems*, 1-7 (2010).
13. Wang, H., Zhou, H., Zhang, Y., Li, D. and Xu, K., Three-dimensional simulation of underfill process in flip-chip encapsulation. *Comp. Fluids*, 44, 187-201 (2011).
14. Hsu, C-C., Chiu, H-S., Yang, W-H. and Chang, R-Y., 3D simulation of fine pitch underfill encapsulation. *Proc. 2010 5th Inter. Microsystems, Packaging, Assembly and Circuits Technol. Conf., and Inter. 3D IC Conf.*, 1-3 (2010).
15. Wenzhong, L. and Xiuli, Y., Flip-chip micro-thermal stress simulation in underfill process. *Proc. 2007 2nd IEEE Inter. Conf. on Nano/Micro Engineered and Molecular Systems*, 1-12 (2007).
16. Wan, J.W., Zhang, W.J. and Bergstrom, D.J., Recent advances in modeling the underfill process in flip-chip packaging. *Microelectron J.,* 38, 67-75 (2007).